InP HBT Wafers: Next-generation materials and technology for high-speed, low-power applications.

Specifications

- 50, 75, and 100 mm
- Carbon-doped InGaAs
- MOCVD production
- Digital and power applications

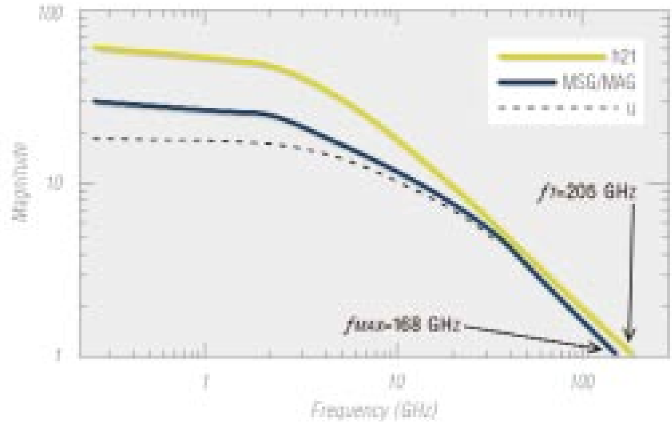
Features and Performance

- InP emitter
- Carbon doping for high reliability
- SHBT and DHBT
  - InGaAsP capability for advanced DHBT structures
  - Graded-base for higher gain and speed performance
- Quick-lot HBT fab and characterization available for maximum yield and quality

EpiWorks offers customers high-level interaction with leading researchers, next-generation GaAs and InP materials technology, device expertise, and a high-yield, reliable product. In addition to our quality EpiHBT™ wafers, EpiWorks also offers a range of products featuring advanced material systems for wireline and wireless applications, including our EpiDetector™, EpiFET™, and EpiLaser™ lines.

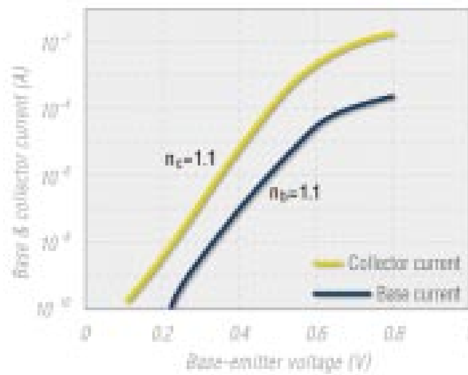
Designed to meet the demands of tomorrow's high-speed 3G wireless and OC-768 networking technologies, Epiworks' InP heterojunction bipolar transistors (HBT) combine high-frequency performance with ultra-low power consumption. Manufacturer of the world's first 100 mm carbon-doped InP HBTs, EpiWorks continues to innovate by delivering advanced DHBTs and graded-base HBTs, in addition to our leading SHBTs.

Figure of merit extrapolation



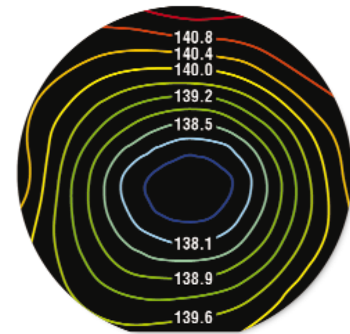
High-frequency performance for a small-area HBT with a 2500 Angstrom collector and a 600 Angstrom base, showing f_t > 200 GHz and f_{max} > 160 GHz.

Gummel plot for InP/InGaAs SHBT



InP/InGaAs SHBT with a 60 x 60 μm² emitter fabricated at EpiWorks on a 100 mm substrate.

Resistivity map for a 100 mm carbon-doped InGaAs layer



Carbon-doped InGaAs layer with typical uniformity of less than 3%.

EpiWorks characterization of InP HBT wafers

Parameter	*Measurement technique*	*Standard tolerance of specified value*
Sheet resistance	Contactless resistivity	±5%
Layer thickness	Profilometer, X-ray diffraction	±10%
Carrier concentration	Hall measurement	±10%
Large-area device data (Beta, R_{sb}, R_{ese}, V_{be}, BV_{ceo}, BV_{ebo}, BV_{cbo}, n_c, n_b)	Full wafer, large-area device process/test	—
Defect density (0.5 to 25 μm²)	Surfscan	<50 cm⁻²

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